REMARKS

Reconsideration of the present application is respectfully requested. Claims 2-4 and 18 have been canceled. Claims 1, 5, 13, 15, 24, 25 and 30 have been amended. No new matter has been added.

Claims 7, 25, 30 and 31 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 15, 16, 18-20, 23, 24, 26, 29 and 32 stand rejected under 35 U.S.C. § 102(e) based on U.S. Patent no. 6,534,726 of Okada et al. ("Okada"). Claims 1, 2, 6, 8, 12, 14, 17 and 27 stand rejected under 35 U.S.C. § 103(a) based on Okada. Claims 3-5, 9-11, 21, 22 and 28 stand rejected under 35 U.S.C. § 103(a) based on Okada in view of U.S. Patent no. 5,222,014 of Lin et al. ("Lin").

The present application includes four independent claims, i.e., claims 1, 8, 15 and 23.

Claim 1

Claim 1, as amended, recites:

> 1. (Currently amended) A method comprising:
> creating a plurality of rows of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate;
> forming a conductive layer on the first surface and on the second surface;
> forming a conductive path through each of the via holes from the first surface to the second surface;
> severing the substrate through each row of via holes and between each row of via holes along a coordinate axis, to produce a plurality of elongate substrate members; and
> affixing two or more of the elongate substrate members together **in an edgewise orientation** to form an interposer with a

plurality of conductive vias **arranged in a two-dimensional array.** (Emphasis added).

Claim 1 has been amended to incorporate limitations similar to those in dependent claim 3 (canceled). Claim 1 was rejected under 35 U.S.C. § 103(a) based on Okada, while claim 3 was rejected under § 103(a) based on Okada in view of Lin.

Okada and Lin do not disclose or suggest, either individually or in combination, affixing two or more of the elongate substrate members together in an edgewise orientation to form an interposer with a plurality of conductive vias arranged in a two-dimensional array. The Examiner admits that "Okada does not appear to explicitly disclose affixing two or more of the elongate substrate members together to form an interposer . . . configured with an array of via holes" (Office Action, pp. 9-10). However, the Examiner contends that the claimed invention feature would be obvious in view of Lin, particularly Lin's disclosure at col. 3, lines 1-26; col. 3 line 58 to col. 2 line 59; col. 5, lines 29-31 and col. 6 lines 22-59 (Office Action, p. 10).

Applicants respectfully disagree. Okada discloses a technique for producing a module substrate onto which an electronic component can be mounted, and which can be mounted to a motherboard. The substrate includes a number of through holes that can be filled with a conductive material. Lin, on the other hand, discloses a multi-chip module (MCM), the different layers of which are stacked over each other. For example, in Fig. 1 of Lin, semiconductor die 10 is sandwiched vertically between substrates 12 and 20.

Assuming *arguendo* the teachings of Okada and Lin can even be combined, at most such combination would suggest stacking Okada's substrates on top of each other, not connecting them edgewise to form a two-dimensional array of conductive vias, as recited in claim 1. There is absolutely no teaching or suggestion in Okada or Lin, or in their combination, to affix together two or more elongate substrate members (constructed as recited in claim 1) in an edgewise orientation to form an interposer that has an array of conductive vias.

Furthermore, there is no suggestion in either Okada or Lin as to why an edgewise configuration such as recited in claim 1 would be desirable. Note that the affixing operation, as recited in claim 1, is done specifically for the purpose of forming a two-dimensional array of vias; in contrast, the stacking of layers in Lin is done to conserve space on the motherboard (see Lin at col. 3, lines 58-62). In fact, it is entirely possible in Lin (though not explicitly stated) that the contacts on each of the substrate layers 12 and 20 already are configured in two-dimensional arrays prior to the stacking of layers.

Therefore, the invention as set forth in claim 1 is not obvious based on Okada, Lin, or any combination thereof.

Claim 8

Claim 1 stands rejected under 35 U.S.C. § 103(a) based on Okada. Claim 8 provides:

> 8. A method of manufacturing an interposer, the method comprising:
> creating a plurality of rows of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate, the first surface and the second surface

being coated with a conductive material;

forming a conductive layer in each of the via holes to provide a conduction path through each of the via holes from the conductive material on the first surface to the conductive material on the second surface;

selectively removing some of the conductive material from the first surface and the second surface to form a plurality of traces on the first surface and the second surface, each trace in electrical contact with the conductive layer in at least one of the via holes; and

severing the substrate to produce a plurality of individual substrate members, by cutting the substrate through the middle of the via holes in each row of via holes **and between each row of via holes** along a particular axis.
(Emphasis added.)

Claim 8 has not been amended, because Okada and Lin do not disclose or suggest a method as recited in claim 8, either individually or in combination. In particular, neither Okada nor Lin discloses or suggests severing the substrate to produce a plurality of individual substrate members, by cutting the substrate through the middle of the via holes in each row of via holes and between each row of via holes along a particular axis. This manner of severing results in the creation of elongate members and facilitates the subsequent affixing of the elongate members together to form a two-dimensional array of contacts (although the affixing operation is not recited in claim 8).

Okada only discloses severing the substrate through the middle of a row of through holes, but not between rows of through holes. Furthermore, Okada provides no motivation as to why it would be desirable to also sever the substrate between rows of through holes; in fact, it is not even apparent how that would be possible in Okada, given the shape and configuration of the substrates 11, 21 in

Okada. Likewise, Lin also does not suggest the manner of severing a substrate as recited in claim 8.

Therefore, the invention as set forth in claim 8 is not obvious based on Okada, Lin, or any combination thereof.

Claim 15

Claim 15 stands rejected under 35 U.S.C. § 102(e) based on Okada. Claim 15, as amended, provides:

> 15. (Currently amended) A method of manufacturing an interposer, the method comprising:
> creating a plurality of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate;
> creating a solid conductive column through each of the via holes, the conductive column forming an electrical path from the first surface to the second surface; and
> **forming grooves** in the first surface and the second surface of the substrate **between the via holes**.
> (Emphasis added.)

Okada does not disclose or suggest such a method. In particular, Okada does not disclose or suggest forming grooves in the first surface and the second surface of the substrate between the via holes. On p. 4 of the Office Action the Examiner contends that Okada discloses such an operation as "forming grooves 53 in the first surface and the second surface between the via holes." Applicant respectfully disagrees.

The grooves 53 are shown in Fig. 16 of Okada and are described at col. 11, lines 12-14 as follows: "End-face through holes 52 are provided on the end-faces 51C of the substrate 51. End-face through-hole 52 comprises an end-face opening groove 53, an end-face electrode 54, and a back-surface electrode 56

which will be described later" (emphasis added). Thus, a groove 53 clearly is part of (inside) a through-hole 52; it is not between through-holes or via holes, as recited in claim 15.

Furthermore, claim 15 requires that the via holes are formed from the first surface to the second surface, but that the grooves are formed in the first and second surfaces. To read Okada on claim 15, therefore, the first and second surfaces would have to be the front surface 51A and back surface 51B of the substrate 51 (referring, for example, to Fig. 16 of Okada). However, such a reading does not work, because the grooves 53 are not formed in the front or back surfaces 51A and 51B of the substrate 51, they are formed in the end-faces 51C (edges) of the substrate 51, which are perpendicular to the front or back surfaces 51A and 51B (col. 11, lines 12-14; Fig. 16). Therefore, Okada fails to read on claim 15.

Therefore, the invention as set forth in claim 8 is not anticipated or obvious based on Okada.

Claim 23

Claim 23 includes limitations substantially similar to those discussed above with regard to claim 15. Therefore, claim 23 is also patentably distinguishable from the cited art for essentially the same reasons as claim 15.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding

any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Conclusion

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,
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